ABSTRACT

A method for designing a semiconductor device includes receiving a net list of a semiconductor device, temporarily locating a plurality of functional blocks within a layout area of the semiconductor device and dividing a logic area of the semiconductor device into a plurality of rectangular areas and computing a predicted value of a utilization rate of the logic area and a predicted value of a wiring length of the semiconductor device based on a data base regarding a semiconductor device designed previously and the semiconductor device and the net list of the semiconductor device. The method also includes locating, dividing and computing when the predicted value of the utilization rate of the logic area of the semiconductor device does not satisfy a predetermined condition, outputting floor plan information for allocating the plurality of functional blocks basic cells and wiring within the logic area of the semiconductor device when the predicted value of the utilization rate of the logic area satisfies the predetermined condition and outputting the predicted value of the wiring length of the semiconductor device.